CLAIMS:

1. A trench MOSFET device comprising:

a substrate of a first conductivity type;

an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial region from an upper surface of said epitaxial layer;

an insulating layer lining at least a portion of said trench;

a conductive region within said trench adjacent said insulating layer;

a doped region of said first conductivity type formed within said epitaxial layer between a bottom portion of said trench and said substrate, said doped region having a majority carrier concentration that is lower than that of said substrate and higher than that of said epitaxial layer;

a body region of a second conductivity type formed within an upper portion of said epitaxial layer and adjacent said trench, said body region extending to a lesser depth from said upper surface of said epitaxial layer than does said trench; and

a source region of said first conductivity type formed within an upper portion of said body region and adjacent said trench.

2. The trench MOSFET device of claim 1, wherein said doped region extends more than 50% of the distance from said trench bottom to said substrate.

3. The trench MOSFET device of claim 2, wherein said doped region spans 100% of the distance from said trench bottom to said substrate.

4. The trench MOSFET device of claim 1, wherein said first conductivity type is n-type conductivity and said second conductivity type is p-type conductivity.

5. The trench MOSFET device of claim 4, wherein said doped region is doped with phosphorous.

6. The trench MOSFET device of claim 4, wherein said substrate is an N+ substrate, said epitaxial layer is an N- epitaxial layer, said doped region is an N region, said body region is a P region, said source region is an N+ region, and.

7. The trench MOSFET device of claim 1, wherein said trench MOSFET device is a silicon device.

8. The trench MOSFET device of claim 7, wherein said first insulating layer is a silicon oxide layer.

9. The trench MOSFET device of claim 7, wherein the conductive region is a doped polycrystalline silicon region.

10. The trench MOSFET device of claim 1, wherein the doped region ranges from 1 to 6 microns in thickness.

11. The trench MOSFET device of claim 4, wherein the doped region has a net n-type carrier concentration ranging from 1 $x10^{18}$ to 5 $x10^{19}$ cm^{-3}.

12. The trench MOSFET device of claim 1, wherein said trenches define a plurality of square-shaped or hexagonal-shaped MOSFET cells.

13. A trench MOSFET device comprising:

a silicon substrate of n-type conductivity;

a silicon epitaxial layer of n-type conductivity over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial region from an upper surface of said epitaxial layer;

a silicon oxide insulating layer lining at least a portion of said trench;

a doped polycrystalline silicon region within said trench adjacent said silicon oxide layer;

a doped region of n-type conductivity provided between a bottom portion of said trench and said substrate, said doped region having a majority carrier concentration that is lower than that of said substrate and higher than that of said epitaxial layer;

a body region of p-type conductivity formed within an upper portion of said epitaxial layer and adjacent said trench, said body region extending to a lesser depth from said upper surface of said epitaxial layer than does said trench; and

a source region of n-type conductivity formed within an upper portion of said body region and adjacent said trench.

14. The trench MOSFET device of claim 13, wherein said doped region spans 100% of the distance from said trench bottom to said substrate.

15. The trench MOSFET device of claim 13, wherein said doped region is doped with phosphorous.

16. The trench MOSFET device of claim 13, wherein the doped region ranges from 1 to 6 microns in thickness.

17. The trench MOSFET device of claim 13, wherein the doped region has a net n-type carrier concentration ranging from 1 $x10^{18}$ to 5 $x10^{19}$ cm^{-3}.

18. A method of forming a trench MOSFET device comprising:

providing a substrate of a first conductivity type;

depositing an epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

etching a trench extending into said epitaxial region from an upper surface of said epitaxial layer, said trench extending to a greater depth from said upper surface of said epitaxial layer than does said body region;

forming a doped region of said first conductivity type between a bottom portion of said trench and said substrate, said doped region having a majority carrier concentration that is lower than that of said substrate and higher than that of said epitaxial layer;

forming an insulating layer lining at least a portion of said trench;

forming a conductive region within said trench adjacent said insulating layer; and

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench.

19. The method of claim 18, wherein said step of forming said doped region comprises:
(a) implanting a dopant of said first conductivity type into said epitaxial region; and
(b) diffusing dopant of said first conductivity type at elevated temperature.

20. The method of claim 19, wherein said dopant is diffused until the doped region spans more than 50% of the distance from said trench bottom to said substrate.

21. The method of claim 19, wherein said dopant is diffused until the doped region spans 100% of the distance from said trench bottom to said substrate.

22. The method of claim 19, wherein said first conductivity type is n-type conductivity and said second conductivity type is p-type conductivity.

23. The method of claim 22, wherein said dopant is phosphorous.

24. The method of claim 18, wherein said steps of forming said trenches and forming said doped region comprise: (a) forming a trench mask on said epitaxial layer; (b) etching said trench through said trench mask; (c) implanting a dopant of said first conductivity type through said trench mask; and (c) diffusing said dopant of said first conductivity type at elevated temperature.

25. The method of claim 24, wherein said elevated temperature is provided by a step in which a sacrificial oxide is grown along walls of said trench.

26. The method of claim 18, wherein said trench MOSFET device is a silicon device.

27. The method of claim 18, further comprising:

forming a metallic drain contact adjacent said semiconductor substrate,

forming a metallic source contact adjacent an upper surface of said source region, and

forming a metallic gate contact adjacent an upper surface of said conductive region remote from said source region.